CLAIM AMENDMENTS

1. (Original) A method usable with a memory device, comprising: receiving a data strobe signal from a memory bus;

capturing data associated with a write command from the memory bus in synchronization with the data strobe signal;

performing a column redundancy check in response to an address associated with the write command; and

synchronizing the beginning of an internal write operation to a memory cell array of the memory device to a clock signal.

2.-36. (Cancelled)

- 37. (New) A method usable with a memory device, comprising:

 performing a column redundancy check; and

 synchronizing the beginning of an internal write operation to a memory cell array of the

 memory device to a clock signal.
- 38. (New) The method of claim 37, wherein the internal write operation begins on an edge of the clock signal.
- 39. (New) The method of claim 37, further comprising: providing column select signals to the memory cell array in synchronization with the clock signal.
- 40. (New) The method of claim 39, wherein the providing of the column select signals comprises:

latching the column select signals synchronously with an edge of the clock signal.

- 41. (New) The method of claim 39, wherein the latching of the column select signals comprises asserting a column address trap signal synchronously with the edge of the clock signal.
- 42. (New) The method of claim 37, wherein the column redundancy check is performed beginning on a first edge of the clock signal and the providing of the column select signals begins on another edge of the clock signal.
 - 43. (New) A method usable with a memory device, comprising:

providing column select signals indicative of a column address to a memory cell array of the memory device; and

performing a column redundancy check prior to the initiation of the providing of the column select signals.

- 44. (New) The method of claim 43, wherein the providing of the column select signals comprises latching the column select signals synchronously with an edge of a clock signal.
 - 45. (New) The method of claim 44, further comprising:

latching data associated with a write command in response to a data strobe signal, wherein the latching of the column select signals comprises asserting a column address trap signal synchronously with the edge of the clock signal.

- 46. (New) The method of claim 43, wherein the performing of the column redundancy check begins on a first edge of a clock signal and the providing of the column select signals begins on another edge of the clock signal.
- 47. (New) The method of claim 46, wherein said another edge comprises the next successive edge of the clock signal after the first edge.

- 48. (New) The method of claim 43, further comprising: asserting another signal to equalize a data I/O line of the memory device for a first time interval that begins after the providing of the column select signals.
 - 49. (New) The method of claim 48, further comprising: deasserting said another signal to terminate the first time interval; and beginning an internal read operation after the deassertion of said another signal.
- 50. (New) The method of claim 49, further comprising: asserting said another signal after the beginning of an internal read operation for a second time interval less than the first time interval.
- 51. (New) The method of claim 43, wherein the memory device comprises a double data rate (DDR) synchronous dynamic random access memory (SDRAM).
 - 52. (New) A memory device comprising:
 - a memory cell array;
- a first circuit to perform a column redundancy check in response to a decoded address; and
- a second circuit to synchronize an initiation of an internal write operation to the memory cell array with a clock signal.
- 53. (New) The memory device of claim 52, wherein the second circuit synchronizes the initiation of an internal write operation to an edge of the clock signal.
- 54. (New) The memory device of claim 52, wherein the first circuit further provides column select signals to the memory cell array in synchronization with the clock signal.
- 55. (New) The memory device of claim 54, wherein the first circuit latches the column select signals synchronously with an edge of the clock signal.

- 56. (New) The memory device of claim 55, wherein the second circuit pulses a column address trap signal synchronously with an edge of the clock signal, and the first circuit latches the column select signals in response to a pulse of the column address trap signal.
- 57. (New) The memory device of claim 52, wherein the first circuit performs the column redundancy check beginning on a first edge of a clock signal and provides the column select signals beginning on another edge of the clock signal.
 - 58. (New) A memory device comprising: a memory cell array; an addressing circuit; and

a control circuit to cause the addressing circuit to perform a column redundancy check during a delay to accommodate variations in the timing of a data strobe signal and begin providing column select signals to the memory cell array after performing the column redundancy check.

- 59. (New) The memory device of claim 58, wherein the addressing circuit provides the column select signals by latching the column select signals synchronously with an edge of a clock signal.
- 60. (New) The memory device of claim 59, wherein the addressing circuit latches the column select signals in response to a column address trap signal, and the control circuit asserts column address trap signal synchronously with the edge of the clock signal.
- 61. (New) The memory device of claim 59, wherein the addressing circuit begins performing the column redundancy check on a first edge of the clock signal and begins providing a column select signals on another edge of the clock signal.

- 62. (New) The memory device of claim 61, wherein said another edge comprises the next successive edge of the clock signal after the first edge.
- 63. (New) The memory device of claim 58, wherein the control circuit asserts another signal to equalize data I/O lines coupled to the memory array for a first time interval that begins after the addressing circuit provides column select signals.
- 64. (New) The memory device of claim 58, wherein the memory device comprises a double data rate (DDR) synchronous dynamic random access memory (SDRAM).
 - 65. (New) A computer system comprising:
 - a memory bus;
 - a memory controller coupled to the memory bus;
- a central processing unit to cause the memory controller to furnish signals to the memory bus to cause a memory operation; and
 - a memory device coupled to the memory bus and adapted to:
- establish a predetermined window of time to capture the data, and
 perform a column redundancy check in response to the memory operation during
 the predetermined window of time.
- 66. (New) The computer system of claim 65, wherein the signals include signals that indicate a write command, and the memory device is further adapted to capture said signals that indicate the write command in synchronization with a clock signal and begin an internal write operation to a memory cell array of the memory device in synchronization with the clock signal.
- 67. (New) The computer system of claim 66, wherein the memory device begins performing the column redundancy check on a first edge of the clock signal and begins performing the internal write operation on another edge of the clock signal.
- 68. (New) The computer system of claim 67, wherein said another edge comprises the next successive edge of the clock signal after the first edge.

- 69. (New) The computer system of claim 66, wherein the memory device begins the internal write operation in response to a column address trap signal, and the memory device includes a control circuit to assert the column address trap signal synchronously with the edge of the clock signal.
- 70. (New) The computer system of claim 69, wherein the control circuit asserts another signal to equalize data I/O lines of the memory device for a first time interval that begins after the memory device begins the internal write operation.
- 71. (New) The computer system of claim 65, wherein the memory device comprises a double data rate (DDR) synchronous dynamic random access memory (SDRAM) device.